We Claim:

1. A storage capacitor, comprising:

a lower capacitor electrode;

a storage dielectric; and

an upper capacitor electrode;

at least one of said lower and upper capacitor electrodes being a conductive layer;

a doped layer selected from the group consisting of a SiGe layer, a SiC layer, and a GaAs layer or a doped filling selected from the group consisting of a SiGe filling, a SiC filling, and a GaAs filling disposed between said conductive layer and said storage dielectric; and

wherein a doped SiGe layer is not disposed between said storage dielectric and said upper capacitor electrode.

2. The storage capacitor according to claim 1 configured to form a part of a DRAM memory cell.

3. The storage capacitor according to claim 1, wherein a dopant for said SiGe layer is selected from the group consisting of Al, Ga, In, Tl, B, As, Sb, and P.

4. The storage capacitor according to claim 1, wherein a dopant for said SiC layer is selected from the group consisting of Al, Ga, In, Tl, B, As, Sb, and P.

5. The storage capacitor according to claim 1, wherein said conductive layer is formed of a material selected from the group consisting of metal silicide, metal nitride, metal carbide, WN, WSiN, WC, TiN, TaN, and TaSiN.

6. The storage capacitor according to claim 1, wherein said storage dielectric contains a material selected from the group consisting of silicon nitride, silicon dioxide, silicon oxynitride, metal oxide, aluminum oxide, Pr_2O_3, Nd_2O_3, Al_2O_3 with an addition of Hf, Zr, Y or La.

7. The storage capacitor according to claim 1, wherein said doped layer has a dopant distribution with a gradient.

8. A storage capacitor, comprising:

a lower capacitor electrode;

a storage dielectric; and

an upper capacitor electrode;

at least one of said lower and upper capacitor electrodes being a conductive layer;

a doped layer selected from the group consisting of a SiGe layer, a SiC layer, and a GaAs layer or a doped filling selected from the group consisting of a SiGe filling, a SiC filling, and a GaAs filling disposed on a side of said conductive layer remote from said storage dielectric; and

wherein a doped SiGe layer is not disposed between said storage dielectric and said upper capacitor electrode.

9. The storage capacitor according to claim 8 configured to form a part of a DRAM memory cell.

10. The storage capacitor according to claim 8, wherein a dopant for said SiGe layer is selected from the group consisting of Al, Ga, In, Tl, B, As, Sb, and P.

11. The storage capacitor according to claim 8, wherein a dopant for said SiC layer is selected from the group consisting of Al, Ga, In, Tl, B, As, Sb, and P.

12. The storage capacitor according to claim 8, wherein said conductive layer is formed of a material selected from the

group consisting of metal silicide, metal nitride, metal carbide, WN, WSiN, WC, TiN, TaN, and TaSiN.

13. The storage capacitor according to claim 8, wherein said storage dielectric contains a material selected from the group consisting of silicon nitride, silicon dioxide, silicon oxynitride, metal oxide, aluminum oxide, Pr_2O_3, Nd_2O_3, Al_2O_3 with an addition of Hf, Zr, Y or La.

14. The storage capacitor according to claim 8, wherein said doped layer has a dopant distribution with a gradient.

15. A storage capacitor, comprising:

a conductive layer forming a lower capacitor electrode;

a storage dielectric;

an upper capacitor electrode; and

a doped Si layer disposed between said conductive layer and said storage dielectric.

16. The storage capacitor according to claim 15 configured to form a part of a DRAM memory cell.

17. The storage capacitor according to claim 15, wherein a dopant for said Si layer is selected from the group consisting of Al, Ga, In, Tl, B, As, Sb, and P.

18. The storage capacitor according to claim 15, wherein said conductive layer is formed of a material selected from the group consisting of metal silicide, metal nitride, metal carbide, WN, WSiN, WC, TiN, TaN, and TaSiN.

19. The storage capacitor according to claim 15, wherein said storage dielectric contains a material selected from the group consisting of silicon nitride, silicon dioxide, silicon oxynitride, metal oxide, aluminum oxide, Pr_2O_3, Nd_2O_3, Al_2O_3 with an addition of Hf, Zr, Y or La.

20. The storage capacitor according to claim 15, wherein said Si layer contains a dopant introduced with a gradient.

21. A memory cell, comprising:

a storage capacitor according to claim 1 formed as a trench capacitor with an upper capacitor electrode;

a selection transistor having a source electrode, a drain electrode, a gate electrode, and a conductive channel; and

wherein said upper capacitor electrode is electrically connected to one of said source and drain electrodes.

22. A memory cell, comprising:

a storage capacitor according to claim 8 formed as a trench capacitor with an upper capacitor electrode;

a selection transistor having a source electrode, a drain electrode, a gate electrode, and a conductive channel; and

wherein said upper capacitor electrode is electrically connected to one of said source and drain electrodes.

23. A memory cell, comprising:

a storage capacitor according to claim 15 formed as a trench capacitor with an upper capacitor electrode;

a selection transistor having a source electrode, a drain electrode, a gate electrode, and a conductive channel; and

wherein said upper capacitor electrode is electrically connected to one of said source and drain electrodes.

24. A memory cell, comprising:

a storage capacitor according to claim 1 formed as a stacked capacitor and having the lower capacitor electrode applied on a connection structure;

a selection transistor having a source electrode, a drain electrode, a gate electrode, and a conductive channel; and

wherein said lower capacitor electrode is electrically conductively connected to one of said source and drain electrodes via said connection structure.

25. A memory cell, comprising:

a storage capacitor according to claim 8 formed as a stacked capacitor and having the lower capacitor electrode applied on a connection structure;

a selection transistor having a source electrode, a drain electrode, a gate electrode, and a conductive channel; and

wherein said lower capacitor electrode is electrically conductively connected to one of said source and drain electrodes via said connection structure.

26. A memory cell, comprising:

a storage capacitor according to claim 15 formed as a stacked capacitor and having the lower capacitor electrode applied on a connection structure;

a selection transistor having a source electrode, a drain electrode, a gate electrode, and a conductive channel; and

wherein said lower capacitor electrode is electrically conductively connected to one of said source and drain electrodes via said connection structure.

27. A storage capacitor, comprising:

a lower capacitor electrode;

a storage dielectric; and

an upper capacitor electrode;

at least one of said lower and upper capacitor electrodes being a conductive filling;

a doped layer selected from the group consisting of a SiGe layer, a SiC layer, and a GaAs layer disposed between said conductive filling and said storage dielectric; and

wherein a doped SiGe layer is not disposed between said storage dielectric and said upper capacitor electrode.

28. The storage capacitor according to claim 27 configured to form a part of a DRAM memory cell.

29. The storage capacitor according to claim 27, wherein a dopant for said SiGe layer is selected from the group consisting of Al, Ga, In, Tl, B, As, Sb, and P.

30. The storage capacitor according to claim 27, wherein a dopant for said SiC layer is selected from the group consisting of Al, Ga, In, Tl, B, As, Sb, and P.

31. The storage capacitor according to claim 27, wherein said conductive layer is formed of a material selected from the group consisting of metal silicide, metal nitride, metal carbide, WN, WSiN, WC, TiN, TaN, and TaSiN.

32. The storage capacitor according to claim 27, wherein said storage dielectric contains a material selected from the group consisting of silicon nitride, silicon dioxide, silicon oxynitride, metal oxide, aluminum oxide, Pr_2O_3, Nd_2O_3, Al_2O_3 with an addition of Hf, Zr, Y or La.

33. The storage capacitor according to claim 27, wherein said doped layer has a dopant distribution with a gradient.

34. A memory cell, comprising:

a storage capacitor according to claim 27 formed as a trench capacitor with an upper capacitor electrode;

a selection transistor having a source electrode, a drain electrode, a gate electrode, and a conductive channel; and

wherein said upper capacitor electrode is electrically connected to one of said source and drain electrodes.

35. A memory cell, comprising:

a storage capacitor according to claim 27 formed as a stacked capacitor and having the lower capacitor electrode applied on a connection structure;

a selection transistor having a source electrode, a drain electrode, a gate electrode, and a conductive channel; and

wherein said lower capacitor electrode is electrically conductively connected to one of said source and drain electrodes via said connection structure.